

Attorney Ref No. 112.P91016

Patent Appl. No. 10/726,641
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FEB 13 2008**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior version, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

Listing of Claims:

1 - 3. (Cancelled)

4. (Currently amended) An apparatus comprising:

an interface ~~circuit device including~~ a board having:a first surface opposite a second surface;

a plurality of first contact receptacles of a first depth on said first surface, at least one of the first contact receptacles including a first end connected to the interface circuit board and a second end to connect to an external device; and

at least two second contact receptacles of a second depth on said first surface, wherein the at least two second contact receptacles include one contact receptacle connected to a first voltage line of a first voltage level, and another contact receptacle connected to a second voltage line of a second voltage level; and

a plurality of pins on said second surface. the plurality of pins adapted to be coupled to integrated circuit contact points, wherein said plurality of pins includes one or more pins that are longer in length than the other pins. and

wherein the second depth is greater than the first depth such that the second contact receptacles are adapted to contact the external device prior to the first contact receptacles contacting said the external device in response to the circuit board being coupled to the external device ~~through the interface device in a direction.~~

Attorney Ref No. 112.P91016

Patent Appl. No. 10/726,641

5 - 27. (Cancelled)

28. (Currently amended) A system, comprising:
a plurality of first pins formed on a first circuit board;
a second circuit board including a first surface opposite and a second surface;
a plurality of first contact points formed on the first surface of the second circuit board to receive the first pins; and
a plurality of second pins formed on the second surface of the second circuit board, the plurality of second pins adapted to be coupled to integrated circuit contact points,
wherein the plurality of first pins includes one or more first pins that are longer in length than the other first pins, or the plurality of second pins includes one or more second pins that are longer in length than the other second pins.

29 - 30. (Cancelled)

31. (Currently amended) A method, comprising:
providing an interface circuit device formed on a board, the interface device including:
a first surface opposite a second surface;
a plurality of first contact receptacles of a first depth on said first surface, at least one of the first contact receptacles including a first end connected to the board and a second end to connect to an external device; and
at least two second contact receptacles of a second depth on said first surface,
wherein the at least two second contact receptacles include one connected to a first voltage line of a first voltage level, and another connected to a second voltage line of a second voltage level;
and
providing a plurality of pins on said second surface, the plurality of pins adapted to be coupled to integrated circuit contact points, wherein said plurality of pins includes one or more pins that are longer in length than the other pins, and wherein the at least two second contact receptacles have with a depth greater than the depth of at least one of the first contact receptacles to discharge electric charges accumulated on the board via the at least two second

Attorney Ref No. 112.P91016

Patent Appl. No. 10/726,641

contact receptacles if the circuit board is coupled to the external device ~~through the interface device;~~

32 – 43. (Cancelled)

44. (Currently amended) A method, comprising:

providing a test device including a first circuit board, the first circuit board including a plurality of first pins;

providing a second board including a first surface opposite and a second surface, the second circuit board including a plurality of first contact points on the first surface to receive the first pins, and a plurality of second pins on the second surface, wherein at least one of the first pins is longer than the other first pins, or at least one of the second pins is longer than that of the other second pins; and

providing a plurality of second contact points on a plurality of integrated circuits to receive the second pins to discharge electric charges accumulated on a third circuit board on which the integrated circuits are formed if the first pins are coupled to the first contact points and the second pins to the second contact points;

45 – 47. (Cancelled)

48. (Currently amended) A system, comprising:

a plurality of first pins formed on a first circuit board;

a second circuit board including a first surface opposite and a second surface;

a plurality of contact receptacles formed on the first surface of the second circuit board to receive the first pins; and

a plurality of second pins formed on the second surface of the second circuit board,

wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, or the plurality of second pins includes one or more second pins that are longer in length than the other second pins.

*Attorney Ref No. 112.P91016**Patent Appl. No. 10/726,641*

49 (Previously Presented) The apparatus of claim 48, wherein the plurality of second pins are adapted to be coupled to integrated circuit contact points.

50. (Previously Presented) The apparatus of claim 48, wherein all of the first pins have equal lengths.

51-53. (Cancelled)

54. (Currently amended) A detecting system, comprising:
a plurality of first pins formed on a test head;
an interconnect circuit board including a first surface opposing and a second surface;
a plurality of contact receptacles formed on the first surface of the interconnect circuit board to receive the first pins; and
a plurality of second pins formed on the second surface of the interconnect circuit board, wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, so that the one or more contact receptacles are adapted to contact the first pins prior to the other contact receptacles contacting the first pins in response to the test head being coupled to the interconnect circuit board.

55-59. (Cancelled)

60. (Currently amended) A method, comprising:
arranging a test head having a plurality of first pins adjacent to an interconnect circuit board that includes a first surface opposite and a second surface, the first surface including a plurality of contact receptacles, and the second surface including a plurality of second pins; and
coupling the test head to the interconnect circuit board so that the contact receptacles receive the first pins,

wherein the plurality of contact receptacles includes one or more contact receptacles that are deeper than the other contact receptacles, so that the one or more contact receptacles are adapted to contact the first pins prior to the other contact

Attorney Ref No. 112.P91016

Patent Appl. No. 10/726,641

receptacles contacting the first pins in response to the test head being coupled to the interconnect circuit board.

61. (Previously Presented) The method of claim 60, further comprising connecting the second pins to a board that includes integrated circuits.

62-64. (Cancelled)

65. (Currently amended) An apparatus, comprising:

a circuit board for an integrated circuit tester, the circuit board including a surface having a plurality of contact pins of a first length and at least one contact pin of a second length longer than the first length;

a second circuit board including a first surface opposite and a second surface;

a plurality of first contact points formed on the first surface of the second circuit board to receive the contact pins; and

a plurality of second pins formed on the second surface of the second circuit board, the plurality of second pins adapted to be coupled to integrated circuit contact points.

66. (Previously Presented) The apparatus of claim 65, wherein the board comprises one of an interface board or an interconnect board.

67. (Previously Presented) The apparatus of claim 65, wherein the plurality of contact pins of a first length and the at least one contact pin of a second length comprise pogo pins.

68. (Previously Presented) The apparatus of claim 65, wherein the plurality of contact pins of a first length are adapted to contact input/output terminals of an integrated circuit mounted on the second board, and wherein the at least one contact pin of the second length is adapted to discharge current from the second board.

69. (Previously Presented) The apparatus of claim 65, wherein the plurality of contact pins of the first length are adapted to contact contact points of the second board, and wherein the

*Attorney Ref No. 112.P91016**Patent Appl. No. 10/726,641*

at least one contact pin of the second length is adapted to discharge current from the second board.

70. (Previously Presented) The apparatus of claim 4, wherein the first voltage level is VSS and the second voltage level is VDD or VCC.

71. (Previously Presented) The apparatus of claim 31, wherein the first voltage level is VSS and the second voltage level is VDD or VCC.

72. (New) The apparatus of claim 4, wherein the first surface and the second surface of the interface circuit board are parallel to one another and able to connect the external device and the integrated circuit contact points, the external device and the integrated circuit contact points being parallel to one another when connected to one another via the interface circuit board.